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☐	L11	L9 and right?side	1
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☐	L7	L6 and (li or L2)	158
☐	L6	L4 and bit near (test or clear or set)	557
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☐	L5	L4	3
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L4	L3 and RISC and compiler	840
☐	L3	bit near (operation or instruction)	19300
		DB=PGPB,USPT,USOC; PLUR=YES; OP=ADJ	
☐	L2	(712/200 |712/201 |712/202 |712/203 |712/204 |712/205 |712/206 |712/207 |712/208 |712/209 |712/210 |712/211 |712/212 |712/213 |712/214 |712/215).ccls.	3077
☐	L1	(717/106 |717/107 |717/136 |717/137 |717/138 |717/139 |717/140 |717/141 |717/142 |717/143 |717/144 |717/145 |717/146 |717/147 |717/148 |717/149 |717/150 |717/151 |717/152 |717/153 |717/154 |717/155 |717/156 |717/157 |717/158 |717/159 |717/160 |717/161).ccls.	3304

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» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **A 32-bit microprocessor for Smalltalk**
Pendleton, J.M.; Kong, S.I.; Brown, E.W.; Dunlap, F.; Marino, C.; Ungar, D.M.; Patterso D.A.;
Solid-State Circuits, IEEE Journal of
Volume 21, Issue 5, Oct 1986 Page(s):741 - 749
AbstractPlus | Full Text: PDF(1400 KB) IEEE JNL

2. **Alpha architecture: Hardware implementation and software programming implica**
Meyer, D.;
Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proceedings., International Conference on
11-14 Oct. 1992 Page(s):4 - 5
AbstractPlus | Full Text: PDF(128 KB) IEEE CNF

3. **A high-performance microarchitecture with hardware-programmable functional u**
Razdan, R.; Smith, M.D.;
Microarchitecture, 1994. MICRO-27. Proceedings of the 27th Annual International Sym
30 Nov.-2 Dec. 1994 Page(s):172 - 180
AbstractPlus | Full Text: PDF(1008 KB) IEEE CNF

4. **An efficient compiler technique for code size reduction using reduced bit-width I**
Halambi, A.; Shrivastava, A.; Biswas, P.; Dutt, N.; Nicolau, A.;
Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings
4-8 March 2002 Page(s):402 - 408
AbstractPlus | Full Text: PDF(419 KB) IEEE CNF

Terms used **RISC compiler bit operation expression** Found **35** of **153,034**

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Relevance scale

1 Session S6.2: compilers and program analysis: Experience with a retargetable compiler for a commercial network processor

Jinhwan Kim, Sungjoon Jung, Yunheung Paek, Gang-Ryung Uh

October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available: pdf(275.87 KB) Additional Information: full citation, abstract, references, citings, index terms

The Paion PPII network processor is designed to meet the growing need for new high bandwidth network equipment. In order to rapidly reconfigure the processor for frequently varying internet services and technologies, a high performance compiler is urgently needed. Albeit various code generation techniques have been proposed for DSPs or ASIPs, we experienced these techniques are not easily tailored towards the target Paion PPII processor due to striking architectural differences. First, we will s ...

Keywords: compiler, network processor, non-orthogonal architecture

2 Specifying representations of machine instructions

Norman Ramsey, Mary F. Fernández

May 1997 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 19 Issue 3

Full text available: pdf(320.62 KB) Additional Information: full citation, abstract, references, citings, index terms

We present SLED, a specification language for Encoding and Decoding, which describes, abstract, binary, and assembly-language representations of machine instructions. Guided by a SLED specification, the New Jersey Machine-Code Toolkit generates bit-manipulating code for use in applications that process machine code. Programmers can write such applications at an assembly language level of abstraction, and the toolkit enables the applications to recognize and emit the binary representations u ...

Keywords: compiler generation, decoding, encoding, machine code, machine description, object code, relocation

3 Simulation and architecture evaluation: Vector vs. superscalar and VLIW architectures for embedded multimedia benchmarks

Christoforos Kozyrakis, David Patterson

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.34 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Multimedia processing on embedded devices requires an architecture that leads to high performance, low power consumption, reduced design complexity, and small code size. In this paper, we use EEMBC, an industrial benchmark suite, to compare the VIRAM vector architecture to superscalar and VLIW processors for embedded multimedia applications. The comparison covers the VIRAM instruction set, vectorizing compiler, and the prototype chip that integrates a vector processor with DRAM main memory.We de ...

4 Fast compilation for pipelined reconfigurable fabrics

Mihai Budiu, Seth Copen Goldstein

February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**

Full text available: pdf(2.03 MB) Additional Information: full citation, references, citings, index terms

5 VISA: A variable instruction set architecture

Alessandro De Gloria

May 1990 **ACM SIGARCH Computer Architecture News**, Volume 18 Issue 2

Full text available: pdf(468.19 KB) Additional Information: full citation, abstract, index terms

This paper presents an instruction coding technique that allows to reduce the instruction width without limiting the exploitation of the machine resources. This result can be obtained by a dynamic instruction coding managed by the compiler.The technique has been applied to a VLIW-structured machine. The machine has an instruction width of 32 bits, while the number of bits needed to code all the functions the machine can perform in a cycle is 98.

6 Initial results on the performance and cost of vector microprocessors

Corinna G. Lee, Derek J. DeVries

December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.73 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Increasingly wider superscalar processors are experiencing diminishing performance returns while requiring larger portions of die area dedicated to control rather than datapath. As an alternative to using these processors to exploit parallelism effectively, we are investigating the viability of using single-chip vector microprocessors. This paper presents some initial results of our investigation where we compare the performance and cost of vector microprocessors to that of aggressive, out-of-or ...

7 APRIL: a processor architecture for multiprocessing

Anant Agarwal, Beng-Hong Lim, David Kranz, John Kubiatowicz

May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture**, Volume 18 Issue 3

Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings, index terms

Processors in large-scale multiprocessors must be able to tolerate large communication latencies and synchronization delays. This paper describes the architecture of a rapid-context-switching processor called APRIL with support for fine-grain threads and synchronization. APRIL achieves high single-thread performance and supports virtual

dynamic threads. A commercial RISC-based implementation of APRIL and a run-time software system that can switch contexts in about 10 cycles is described. Me ...

8 LISP on a reduced-instruction-set-processor

Peter Steenkiste, John Hennessy

August 1986 **Proceedings of the 1986 ACM conference on LISP and functional programming**

Full text available: pdf(953.13 KB) Additional Information: full citation, references, citings

9 Value-based clock gating and operation packing: dynamic strategies for improving processor power and performance

David Brooks, Margaret Martonosi

May 2000 **ACM Transactions on Computer Systems (TOCS)**, Volume 18 Issue 2

Full text available: pdf(210.51 KB) Additional Information: full citation, abstract, references, citings, index terms

The large address space needs of many current applications have pushed processor designs toward 64-bit word widths. Although full 64-bit addresses and operations are indeed sometimes needed, arithmetic operations on much smaller quantities are still more common. In fact, another instruction set trend has been the introduction of instructions geared toward subword operations on 16-bit quantities. For examples, most major processors now include instruction set support for multimedia operation ...

10 Optimal integrated code generation for clustered VLIW architectures

Christoph Kessler, Andrzej Bednarski

June 2002 **ACM SIGPLAN Notices , Proceedings of the joint conference on Languages, compilers and tools for embedded systems: software and compilers for embedded systems**, Volume 37 Issue 7

Full text available: pdf(227.07 KB) Additional Information: full citation, abstract, references, index terms

In contrast to standard compilers, generating code for DSPs can afford spending considerable resources in time and space on optimizations. Generating efficient code for irregular architectures requires an integrated method that optimizes simultaneously for instruction selection, instruction scheduling, and register allocation.We describe a method for fully integrated optimal code generation based on dynamic programming. We introduce the concept of *residence classes* and *space profiles*

Keywords: *dynamic programming, instruction scheduling, instruction selection, integrated code generation, register allocation, space profile*

11 Computation techniques for FPGAs: An FPGA-based VLIW processor with custom hardware execution

Alex K. Jones, Raymond Hoare, Dara Kusic, Joshua Fazekas, John Foster

February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**

Full text available: pdf(220.52 KB) Additional Information: full citation, abstract, references, index terms

The capability and heterogeneity of new FPGA (Field Programmable Gate Array) devices continues to increase with each new line of devices. Efficiently programming these devices is increasing in difficulty. However, FPGAs continue to be utilized for algorithms traditionally targeted to embedded DSP microprocessors such as signal and image processing applications.This paper presents an architecture that combines VLIW (Very Large Instruction Word) processing with the capability to introduce applicat ...

Keywords: NIOS, VLIW, compiler, kernels, parallelism, synthesis

12 Multimedia and graphics: Enhancing loop buffering of media and telecommunications applications using low-overhead predication

John W. Sias, Hillery C. Hunter, Wen-mei W. Hwu

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings

Publisher Site

Media- and telecommunications-focused processors, increasingly designed as deeply pipelined, statically-scheduled VLIWs, rely on loop buffers for low-overhead execution of simple loops. Key loops containing control flow pose a substantial problem---full predication has a high encoding overhead, and partial predication techniques do not support if-conversion, the transformation of general acyclic control flow into predicated blocks. Using a set of significant media processing benchmarks, drawn fr ...

13 Static single assignment form for machine code

Allen Leung, Lal George

May 1999 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1999 conference on Programming language design and implementation**, Volume 34 Issue 5

Full text available: pdf(1.31 MB) Additional Information: full citation, abstract, references, citings, index terms

Static Single Assignment (SSA) is an effective intermediate representation in optimizing compilers. However, traditional SSA form and optimizations are not applicable to programs represented as native machine instructions because the use of dedicated registers imposed by calling conventions, the runtime system, and target architecture must be made explicit. We present a simple scheme for converting between programs in machine code and in SSA, such that references to dedicated physical registers ...

14 Experience with fine-grain synchronization in MIMD machines for preconditioned conjugate gradient

Donald Yeung, Anant Agarwal

July 1993 **ACM SIGPLAN Notices , Proceedings of the fourth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 28 Issue 7

Full text available: pdf(1.29 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses our experience with fine-grain synchronization for a variant of the preconditioned conjugate gradient method. This algorithm represents a large class of algorithms that have been widely used but traditionally difficult to implement efficiently on vector and parallel machines. Through a series of experiments conducted using a simulator of a distributed shared-memory multiprocessor, this paper addresses two major questions related to fine-grain synchronization in the cont ...

15 The KScalar simulator

J. C. Moure, Dolores I. Rexachs, Emilio Luque

March 2002 **Journal on Educational Resources in Computing (JERIC)**, Volume 2 Issue 1

Full text available: pdf(493.35 KB) Additional Information: full citation, abstract, references, index terms

Modern processors increase their performance with complex microarchitectural mechanisms, which makes them more and more difficult to understand and evaluate. KScalar is a graphical simulation tool that facilitates the study of such processors. It allows students to analyze the performance behavior of a wide range of processor microarchitectures: from a very simple in-order, scalar pipeline, to a detailed out-of-order,

superscalar pipeline with non-blocking caches, speculative execution, and comp ...

Keywords: Education, pipelined processor simulator

16 High-cost CFD on a low-cost cluster

Thomas Hauser, Timothy I. Mattox, Raymond P. LeBeau, Henry G. Dietz, P. George Huang
November 2000 **Proceedings of the 2000 ACM/IEEE conference on Supercomputing (CDROM)**

Full text available: pdf(4.00 MB) Additional Information: full citation, abstract, references, index terms
Publisher Site

Direct numerical simulation of the Navier-Stokes equations (DNS) is an important technique for the future of computational fluid dynamics (CFD) in engineering applications. However, DNS requires massive computing resources. This paper presents a new approach for implementing high-cost DNS CFD using low-cost cluster hardware. After describing the DNS CFD code DNSTool, the paper focuses on the techniques and tools that we have developed to customize the performance of a cluster ...

17 INSIDE: INstruction Selection/Identification & Design Exploration for Extensible Processors

Newton Cheung, Sri Parameswaran, J?Henkel
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(248.23 KB) Additional Information: full citation, abstract, index terms

This paper presents the INSIDE system that rapidly searchesthe design space for extensible processors, given area and performance constraints of an embedded application, while minimizing the design turn-around-time. Our system consists ofa) a methodology to determine which code segments are mostsuited for implementation as a set of extensible instructions,b) a heuristic algorithm to select pre-configured extensibleprocessors as well as extensible instructions (library), and c)an estimation tool ...

18 HW/SW co-design: Instruction set and functional unit synthesis for SIMD processor cores

Nozomu Togawa, Koichi Tachikake, Yuichiro Miyaoka, Masao Yanagisawa, Tatsuo Ohtsuki
January 2004

Full text available: pdf(161.66 KB) Additional Information: full citation, abstract, references
Publisher Site

This paper focuses on SIMD processor synthesis and proposes a SIMD instruction set/functional unit synthesis algorithm. Given an initial assembly code and a timing constraint, the proposed algorithm synthesizes an area-optimized processor core with optimal SIMD functional units. It also synthesizes a SIMD instruction set. The input initial assembly code is assumed to run on a full-resource SIMD processor (virtual processor) which has all the possible SIMD functional units. In our algorithm, we i ...

19 MSIM: an improved microcode simulator

Simeon Simeonov, G. Michael Schneider
June 1995 **ACM SIGCSE Bulletin**, Volume 27 Issue 2

Full text available: pdf(515.55 KB) Additional Information: full citation, index terms

20 Warp: an integrated solution of high-speed parallel computing

S. Borkar, R. Cohn, G. Cox, S. Gleason, T. Gross
November 1988 **Proceedings of the 1988 ACM/IEEE conference on Supercomputing**

Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, references, citings, index terms

iWarp is a system architecture for high speed signal, image and scientific computing. The heart of an iWarp system is the iWarp component: a single chip processor that requires only the addition of memory chips to form a complete system building block, called the iWarp cell. Each iWarp component contains both a powerful computation engine (20 MFLOPS) and a high throughput (320 MBytes/sec), low latency (100-150 ns) communication engine for interfacing with other iWarp cells. Because of its s ...

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32 bit operation
... for application tasks; the system is expected to be compatible with the older **RISC** OS API. ... Newer ARM processors will not support 26 **bit operation**. ...
www.heyrick.co.uk/assembler/32bit.html - 21k - Cached - Similar pages

Introduction of the 64-bit Operating System
... a 32-bit or 64-bit operating system on systems that support 64-**bit operation**, ... The following HP **compiler** products support both 64-bit and 32-bit ...
docs.hp.com/en/B3782-90716/ch02s02.html - 58k - Cached - Similar pages

"Bitslice" DES key search
... necessary to compute DES are well-suited to this kind of single-**bit operation**. ... memory on an Alpha, and the size is similar for other **RISC** CPUs. ...
www.cs.cmu.edu/People/dkindred/des/bitslice.html - 10k - Cached - Similar pages

Efficient C Code For Resource-Constrained Systems
... the other requires that the **compiler** analyse the structure of some **source code** and to ... is likely to be much higer than performing an 8-**bit operation**. ...
www.cyclicode.net/doc/djh1/djh1.html - 51k - Apr 7, 2005 - Cached - Similar pages

EDN - 2002 DSP directory - 4/4/2002 - EDN - CA203797
... device to use a more complex and robust instruction set than a 16-**bit operation** code, ... Support: The ARCtangent **RISC**/DSP comes with RTL **source code**, ...
www.edn.com/article/CA203797.html - Similar pages

EDN - 2003 DSP directory - 4/3/2003 - EDN - CA286246
... Development support: The ARCtangent **RISC**/DSP comes with RTL **source code**, ... the ARChitect tool, MetaWare C/C++ **Compiler** and SeeCode debugger, ...
www.edn.com/article/CA286246.html - Similar pages
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[PPT] R8C/Tiny Series
File Format: Microsoft Powerpoint 97 - View as HTML
... Performance improves (faster) due to Barrel Shifter and 32-**bit operation** ... **RISC** instruction result in bigger code. Small RAM and stack size ...
america.renesas.com/media/ company_info/m16c_seminars_2005/4_R8C.ppt - Similar pages

[PDF] A Survey of Networking/Communication Processors
File Format: PDF/Adobe Acrobat - View as HTML
... **Source Code**. Verilog. **Source Code**. Library. Library. C **compiler**. C **compiler** ... 16 **bit Operation**/sec. 24000M. 12000M. 6000M. Local Storage Memory ...
campuscgi.princeton.edu/~znhuang/mescal/ppt/19.pdf - Similar pages

Processor Integration in a Disk Controller
... We also needed a **compiler** for the processor to compile the C **source code**, ... **compiler** runs in two different modes to handle 16- and 32-**bit operation**. ...
doi.ieeecomputersociety.org/10.1109/40.612221 - Similar pages

[PDF] Microsoft PowerPoint - Software Porting - Rich Brunner.ppt
File Format: PDF/Adobe Acrobat
... Optional REX prefix specifies 64-**bit operation** size override ... Many of the tools in the GNU C **Compiler** suite have new switches ...
www.amd.com/us-en/assets/content_type/ DownloadableAssets/Software_Porting_-_Rich_Brunner.pdf - Similar pages

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1. 32 **bit operation**
   32 **bit operation**. A lot of this information is taken from the ARM assembler manual. I didn't have a 32 bit OS needs ... to see my C **compiler** generate code that depends ...
   www.heyrick.co.uk/assembler/32**bit**.html - 21k - Cached - More from this site

2. Introduction of the 64-bit Operating System
   ... systems that support 64-**bit operation**, with the exception of ... your C or C++ **source code**. These too
   docs.hp.com/en/B3782-90716/ch02s02.html - 59k - Cached - More from this site

3. Linux Today - Linus Torvalds: Linux 2.6.0-test6
   ... libraries, tools plus **source code**, GNU cross-**compiler** instructions, board schematics ... Avoid type wa
   linuxtoday.com/news_story.php3?ltsn=2003-09-28-002-26-NW-KN-DV - 99k - Cached - More from this sit

4. Efficient C Code For Resource-Constrained Systems
   ... obvious how a **compiler** might look at some **source code**, but as ... true everywhere however! Some F
   www.cyclic**ode**.net/doc/djh1/djh1.html - 52k - Cached - More from this site

5. KeepMedia | EDN: 2002 DSP directory
   ... includes an assembler or a **compiler** in the tool set ... than a 16-**bit operation** code, and the 16 ... The
   www.keepmedia.com/pubs/EDN/2002/04/04/241399 - More from this site

6. http://invent9k.external.hp.com/doc/11.00RelNotes
   ... APIs in C and C++ **source code**, scripts, and makefiles ... run on PA-**RISC** 2.0 systems. The **compiler**
   invent9k.external.hp.com/doc/11.00RelNotes - 525k - Cached - More from this site

7. KeepMedia | EDN: 2003 DSP Directory
   ... that include an assembler or **compiler** in the tool set ... ADSP-21xx processors are **source-code**-comp
   www.keepmedia.com/pubs/EDN/2003/04/03/116745 - More from this site

8. Hardware Design:
   ... APPENDIX A - VERILOG **SOURCE CODE** A-1 ... 1-**bit operation** affects / has no affect ... **compiler** o
   www.ee.unb.ca/thesis98/ee4000i/finalreport.html - 115k - Cached - More from this site

9. "Bitslice" DES key search
   ... to this kind of single-**bit operation**. In a bit ... Alpha, and the size is similar for other **RISC** CPUs ... bitsl
   www.cs.cmu.edu/People/dkindred/des/**bit**slice.html - 10k - Cached - More from this site

10. New Product Gallery
    ... stand-alone desktop **source-code** browser. It captures ... a C/C++ **compiler**, an assembler, a linker ...
    www.embedded.com/2000/0011/0011newprod.htm - 94k - Cached - More from this site

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Searching for **PHRASE risc compiler bit operation**.
Restrict to: Header Title Order by: Expected citations Hubs Usage Date Try: Google (CiteSeer) Google (Web) Yahoo! MSN CSB DBLP
No documents match Boolean query. Trying non-Boolean relevance query.
500 documents found. **Order: relevance to query.**

Auto-Configurable Array for GCD Computation (Extended Abstract) - Jebelean (1997) (Correct)
GCD Computation extended abstract Tudor Jebelean **RISC**-Linz A-4232 Hagenberg, Austria Tel: 43 (7236)
Preliminary experiments show that for 100 **bits** a speed-up of 4 over software can be obtained
greatest common divisor is the most complicated **operation** over integers and also the most time consuming
ftp.risc.uni-linz.ac.at/pub/techreports/1997/97-12.ps.gz

Evaluation of Pseudo Vector Processor based on.. - Nakamura.. (1994) (Correct)
architecture. In this paper, HewlettPackard PA-**RISC** 1.1 Architecture [Hew90] is selected as an example
number in our architecture. This is helpful for **compilers** to generate efficient object codes because
is summarized here. Registers: Thirty-two 32-**bit** general registers and thirtytwo 64-**bit**
arch.is.tsukuba.ac.jp/pub/papers/Processor/hicss27.ps.Z

On Using a Manhattan Distance-like Function for Robot Motion.. - Van Geem (1994) (Correct)
Grid in Configuration Space. Carl Van Geem **RISC**-Linz Research Institute for Symbolic Computation
and one at the back. Therefore, the same shift **operations** as in the case of a quadtree hold, but we now
ftp.risc.uni-linz.ac.at/pub/techreports/1994/94-74.ps.gz

Virtual Tasks for the PACLIB Kernel - Schreiner (1994) (Correct) (2 citations)
Kernel Wolfgang Schreiner Wolfgang.Schreiner@**risc**.uni-linz.ac.at Research Institute for Symbolic
t returned by pacVirtual may participate in all **operations** like the handles of result descriptors that are
in pacShell and pacWait consists of a simple test **operation**. We will now discuss some of the consequences
www.risc.uni-linz.ac.at/people/schreine/papers/virtual.ps.gz

Register Allocation Using Lazy Saves, Eager Restores, and .. - Burger, Waddell, Dybvig (1995) (Correct)
Association for Computing Machinery, Inc. Our **compiler** dedicates a set of registers to be used to hold
Liveness information is collected using a **bit** vector for the registers, implemented as an n-**bit**
a deficiency involving short-circuit boolean **operations** within if test expressions. 1 Because tail
ftp.cs.indiana.edu/pub/scheme-repository/doc/pubs/Reg-Alloc-PLDI95.ps.gz

Experience Using an Intermediate Compiler Target Language for.. - Papadopoulos (Correct)
Experience Using an Intermediate **Compiler** Target Language for Parallel Machines George A.
of these computations, even primitive arithmetic **operations** are represented as functions a possible
a different value if they apply the dereferencing **operation** to the node. LetRes represents the computation
www.cs.ucy.ac.cy/M_M.ps.gz

Dynamic Processor Allocation with the Solaris Operating System - Yue (1998) (Correct) (11 citations)
commercial operating system and parallelizing **compiler** and provides further evidence of the performance
Cliffs, New Jersey, 1990. 3] J. Barton and N. **Bit**ar. A scalable multi-discipline, multiple-processor
strategy called gang scheduling [3]The **operation** of this gang scheduling depends on the
ftp-mount.ee.umn.edu/pub/faculty/lilja/papers/llpc-on-solaris.ps

Consortium - Release Date (Correct)
produced 4 5 Using a Back-end in a COSY **Compiler** 4 6 The Machine Specification 4 7 Various levels
block. All PMIR basic block manipulations and **operations** on control graph are target independent
ftp.inria.fr/INRIA/Projects/oscar/FNC-2/publications/pagode.ps.gz

The Nexus Approach to Integrating Multithreading and Communication - Foster (1996) (Correct) (143 citations)
a runtime system called Nexus that is used as a **compiler** target for parallel languages and as a
send/receive communication models, a send **operation** in one process is matched by a receive in
to a thread, or should threads and communication **operations** be decoupled? Should the code executed in
now.cs.berkeley.edu/clumps/jpdc.ps

High Performance Fortran Interfacing to ScaLAPACK - Lorenzo, Müller, Murakami.. (1996) (Correct) (4 citations)
inter-processor communication is generated by the **compiler**. While HPF can ease parallelization of many a FORALL statement to extend Fortran 90 array **operations**, automatic conversion of one data distribution performance based on level-2 and level-3 BLAS **operations** [DDHD88]on the one hand, while ensuring good
www.cscs.ch/Official/TechReports/1996/TR-96-13.ps.gz

Drafting ER and OO Schemas in Prototyping Environments - Meyer, Westerman, Gogolla (1996) (Correct)
The system basically consists of a set of **compilers** written in Prolog which translate data language for arbitrary user-defined data types, **operations**, and predicates having these types as domains. point, real)selectors radius :circle -real **operations** pdist :point x point -real predicates cccut
www.db.informatik.uni-bremen.de/publications/Meyer_1996_DKE.ps.gz

A Short Cut to Deforestation - Gill, Launchbury, Jones (1993) (Correct) (141 citations)
implemented the method in the Glasgow Haskell **compiler**. 1 Introduction Functional programs are often at the end of the list by a given value z. This **operation** is encapsulated by the higher-order function In particular, this leads to constanttime append **operations**. This idea of optimising append using
ftp.dcs.gla.ac.uk/pub/glasgow-fp/papers/deforestation-short-cut.ps.Z

Bibliography of Yale's Functional Programming Research Group (aka.. - Hudak (1994) (Correct)
1991. 91] D. Kranz. ORBIT: An Optimizing **Compiler** For Scheme. PhD thesis, Yale University, [37] J. Guzm'an and P. Hudak. Provably complete **operational** semantics for first-order lazy narrowing.
www.cs.yale.edu/HTML/YALE/CS/haskell/bib.ps

The Measured Network Traffic of Compiler–Parallelized Programs - Peter Dinda (1998) (Correct)
The Measured Network Traffic of **Compiler**-Parallelized Programs Peter A. Dinda Brad M. its connections (a shift pattern.Unlike variable **bit** rate video source, where the periodicity is
reports-archive.adm.cs.cmu.edu/anon/1998/CMU-CS-98-144.ps

Code Scheduling for Multiple Instruction Stream Architectures - Tyson, Farrens (1994) (Correct) (2 citations)
performed are unchanged from standard **RISC** architectures. Additional restrictions must be this level of parallelism. 1. Introduction The **compiler** and code scheduler for a multi-issue Element All instructions in MISC are 32 **bits** in length and have three 6-**bit** source operand
american.cs.ucdavis.edu/publications/IJPP.94.ps

Bootstrapping Higher-Order Program Transformers from.. - Sperber, Glück, Thiemann (1996) (Correct) (3 citations)
form. The latter can serve as the middle end of a **compiler**. The generated transformers are strictly more component. The interpreter tries to perform each **operation** with the static component of the input first
ftp.diku.dk/diku/semantics/papers/D-282.ps.gz

Streaming Prefetch - Temam (1995) (Correct) (4 citations)
May 1991. 11] Dick Pountain. A different Kind of **RISC**. BYTE, August 1994. 12] Alan Smith. Cache of prefetching can be easily obtained from the **compiler**, resulting in nearly no wrong predictions. Even and the address before)plus a number of flag **bits**. Consequently, the table size makes it a costly
ftp.prism.uvsq.fr/pub/reports/1995/1995.029.ps.gz

Mostly-Copying Collection: A Viable Alternative to.. - Smith, Morrisett (1997) (Correct) (4 citations)
USA Abstract. Many high-level language **compilers** generate C code and then invoke a C **compiler** to size of the objects allocated in the block, and a **bit**mask indicating the objects that have been marked. branch, 1 compare, and 1 add. Most of the memory **operations** are related to managing the free list. 1
simon.cs.cornell.edu/home/fms/Papers/mcc.ps.gz

TAU: A Portable Parallel Program Analysis Environment for pC - Bernd Mohr (1994) (Correct) (25 citations)
support variable size problem sets, and portable **compiler** platforms to provide access to multiple parallel with a clean interface to data-parallel style **operations** by simply calling member functions of the base
www.cs.uoregon.edu/research/paracomp/proj/tau/../papers/conpar94.bw.ps.gz

Task-Oriented Generation of Visual Sensing Strategies - Jun Miura (1995) (Correct) (5 citations)
Abstract In vision-guided robotic **operations**, vision is used for extracting necessary

which describes what objects are involved in the **operation**, and how they are assembled. Our method has
1 Introduction In vision-guided robotic **operations**, visual sensing strategies should be planned so
www-cv.ccm.eng.osaka-u.ac.jp/members/jun/psfiles/iccv95.ps.Z

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